

Noah Bean

noahbean3396@gmail.com — (971) 419-0100 — linkedin.com/in/noah-bean — github.com/noahbean33

Education

Oregon State University

Corvallis, OR

B.S. Electrical and Computer Engineering

GPA: 3.81/4.0

Dec 2025

Relevant Coursework: Computer Architecture, Operating Systems, Microcontroller System Design, Digital Signal Processing, Signals & Systems, Computer Networking, Parallel Programming.

Technical Skills

Lab Instrumentation: Oscilloscopes, Logic Analyzers, Spectrum Analyzers, JTAG, Vector Network Analyzers, Digital Multimeters, Signal Generators, Programmable Power Supplies.

Hardware Design: High-speed PCB Layout, Multi-layer Stack-up Design, Differential Pair Routing, Controlled Impedance, Signal Integrity, Power Integrity, EMI/EMC Mitigation, Thermal Stress Profiling.

EDA & Simulation: KiCad, Xilinx Vivado, Cadence Allegro, ModelSim, LTspice.

Languages/Software: Python, C, C++, Verilog, SystemVerilog, MATLAB, x86 Assembly, Bash, Linux, Git.

Protocols & Standards: PCIe, DDR, I2C, SPI, UART.

Professional Experience

Collins Aerospace

Wilsonville, OR

Systems and Electrical Engineering Intern

Jun 2025 – Dec 2025

- **Hardware Validation & Test Automation:** Conducted functional and electrical verification on avionics units using lab instrumentation (oscilloscopes, power supplies). Developed automated test scripts to standardize data collection.
- **Component Reliability & Design Integrity:** Performed electrical derating and stress analysis on flight-critical PCB assemblies. Validated component selections against rigorous design margins to mitigate risks related to thermal limits and voltage stressors.
- **Signal Processing & Hardware Verification:** Implemented and verified digital signal processing algorithms for real-time sensor data acquisition.

Intel Corporation

Hillsboro, OR

Electrical Engineering Intern

Apr 2024 – Sep 2024

- **Silicon Failure Analysis & Hardware Debug:** Conducted root-cause electrical analysis on server-grade CPUs, GPUs, and DDR5 memory. Utilized oscilloscopes and logic analyzers to isolate signal integrity issues and electrical shorts, ensuring High-Volume Manufacturing reliability.
- **Hardware Telemetry & Validation Automation:** Engineered Python-based frameworks to automate the extraction of on-chip telemetry data and hardware logs.
- **Computer Vision for IC Inspection:** Developed a defect detection system for wafer and PCB-level inspection.

Technical Projects

x86 Carrier Board

KiCad, High-Speed Design, DFM

- Designed a 4-layer carrier board for the Intel N100 platform. Managed complex routing for USB 3.0, HDMI, and PCIe differential pairs with strict length-matching and impedance requirements.
- Implemented Power Delivery Network capable of handling transient current spikes and integrated ESD protection and signal conditioning for Gigabit Ethernet and GPIO headers.

FPGA-Based Digital Oscilloscope

Vivado, C

- Architected a digital oscilloscope utilizing a custom-designed analog front-end and Artix-7 FPGA. Developed a high-speed data pipeline using DMA and circular buffers for real-time telemetry capture.
- Engineered embedded C firmware on a MicroBlaze soft-processor to interface with hardware registers, manage trigger logic, and export waveform data via UART.

RV32I RISC-V CPU Core

Verilog, Vivado

- Designed a single-cycle CPU from the ISA spec, including ALU logic, control units, and memory-mapped I/O.
- Validated functionality through self-checking testbenches, ensuring 100% instruction set coverage and proper pipeline timing.